The maximum mark for the examination paper is 60 marks, and the mark obtainable for each part of a question is shown in brackets alongside the question.

Instructions to the candidates:

- This exam measure program competences no. (B2, B3, and B4);
- Clarify your answer with the suitable sketches as you can;
- Please use a pen or heavy pencil to ensure legibility;
- Please attempt all questions.

QUESTION NUMBER ONE [30 MARKS]

1. The state table of a sequential circuit is given in the below figure. [7 Marks]
   (a) Reduce the number of states in the state table and draw the reduced state diagram.
   (b) Starting form state "a", find the output sequence generated with an input 0111001. Repeat the task using the reduced table and comment on the result.

Present state	Next state $x=0$	Next state $x=1$	Output $x=0$	Output $x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

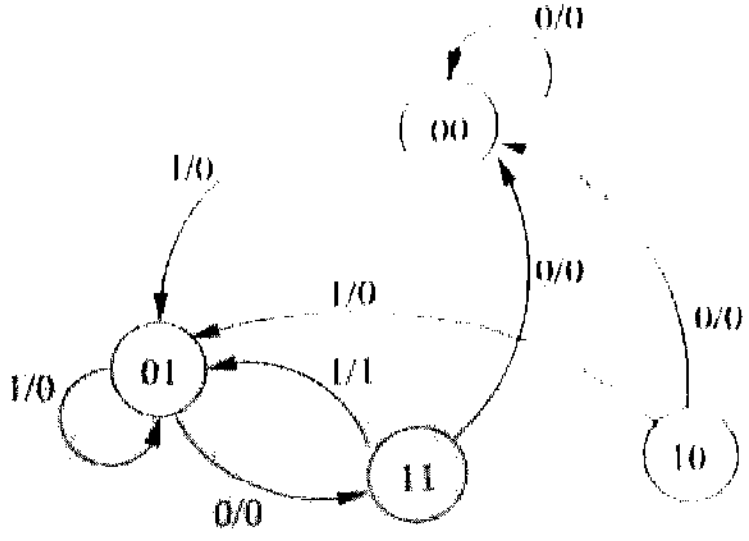
2. Design a synchronous circuit with two JK flip-flops and two inputs E and X. If E=0, the circuit remains in the same state regards less the value of X. When E=1 and X=0, the circuit goes through the state transitions from 00, to 11 to 10 to 01 back to 00 and repeat. When E=1 and X=1, the circuit goes through the state transitions from 00, to 01 to 10 to 11 back to 00 and repeat. [10 Marks]

3. Write the VHDL code for the circuit describes positive edge trigger JK flip-flop. [5 Marks]

4. Develop the logic diagram for a 4-bit universal register which has both the right shift and left shift with parallel load capabilities. The data are effectively shifted one place after a clock pulse arrives. After that, state its function table. [8 Marks]

QUESTION NUMBER ONE [30 MARKS]

1. Consider the following state diagram for a synchronous circuit with one input X and one output Z. The system reads the input X one bit at a time. Draw its circuit implementation using JK flip-flop for Q0, T flip-flop for Q1 and MUX 4x1 for Z. [8 Marks]



2. Construct a positive edge D-flip flop using two MUX 2-to-1 and an inverter. [7 Marks]

3. Design a counter which counts down, with the repeated sequence: 2, 1, 0, when the input to the counter circuit is 1. The counter stays at the same state when the input is 0. The circuit is to be designed by treating the unused states as don't care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states. [Hint: use T flip flops in your design]. [10 Marks]

4. Fill in the timing diagrams for each of the following circuits. [5 Marks]