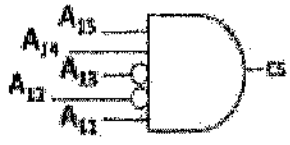
The maximum mark for the examination paper is 60 marks, and the mark obtainable for each part of a question is shown in brackets alongside the question.

Instructions to the candidates:

- This exam measure program competences no. (B2, B3, and B4);
- Clarify your answer with the suitable sketches as you can;
- Please use a pen or heavy pencil to ensure legibility.

QUESTION NUMBER ONE [20 MARKS]

1. What types of connections are common to all memory devices? Assume that the memory system shown below has 16 address lines denoted by A15 to A0.
   a) What is the total size of the memory in the circuit?
   b) What is the range of addresses that can get enabled by the chip select signal? [4 Marks]



2. Design an address decoding logic using MS621000 (128 KB X 8) SRAM, a PLD and an OR gate to interface a total of 1 MB memory system with 80486 μp in the address range that begins at location 02000000H through 020FFFFFH. [8 Marks]
3. Interface 16 KB of RAM to 8086 microprocessor starting at 00000H. Two kinds of chips available are 2KB (4 chips) and 4KB (2 Chips). [8 Marks]

QUESTION NUMBER TWO [20 MARKS]

1. Draw a flowchart that describe the instruction cycle for the different categories of instructions available in the instruction set of the basic computer. [3 Marks]
2. Show the gate structure associated with the control inputs of stop flip flop. [4 Marks]
3. A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. Draw the instruction word format and indicate the number of bits in each part? How many bits are there in the data inputs of the memory? [3 Marks]

4. Explain why each of the following micro-operations cannot be executed during a single clock pulse. Specify a sequence of micro-operations that will perform the operation. [5 Marks]
   a) IR ← M[PC]
   b) AC ← AC + TR
   c) DR ← DR + AC (AC does not change)

5. The operations to be performed with a flip-flop F (not used in the basic computer) are specified by the following register transfer statements:

xT_3:	$F \leftarrow 1$	Set F to 1
yT_1:	$F \leftarrow 0$	Clear F to 0
zT_2:	$F \leftarrow \overline{F}$	Complement F
wT_3:	$F \leftarrow G$	Transfer value of G to F

   Otherwise, the content of F must not change. Draw the logic diagram showing the connections of the gates that form the control functions and the inputs of flip-flop F. Use a JK flip-flop and minimize the number of gates. [5 Marks]

Question number three [20 Marks]

1. Explain the term handshaking as it applies to microprocessor I/O systems (Hint: I expect to see a timing diagram that illustrates the term handshaking). [4 Marks]
2. Draw the functional block diagram of the programmable peripheral interface. Then, explain how is 82C55 configured, if its control register contains 9B h. [6 Marks]
3. Based on the configuration of 82C55 chip, connect 3 LED to port C, blink one LED after another at regular intervals of 1 ms. The 82C55 base address is 04H. [5 Mars]
4. How is the address of the interrupt service routine calculated in vectored interrupts? Briefly illustrate the working operation of power failure detection circuit that causing NMI interrupt when AC power drop out. [5 Marks]

Fetch	$R'T_0$:	$AR \leftarrow PC$
	$R'T_1$:	$IR \leftarrow M[AR]$, $PC \leftarrow PC + 1$
Decode	$R'T_2$:	$D_0, \ldots, D_7 \leftarrow$ Decode $IR(12\text{–}14)$, $AR \leftarrow IR(0\text{–}11)$, $I \leftarrow IR(15)$
Indirect	D_7IT_3:	$AR \leftarrow M[AR]$
Interrupt:		
	$T_0'T_1'T_2'(IEN)(FGI + FGO)$:	$R \leftarrow 1$
	RT_0:	$AR \leftarrow 0$, $TR \leftarrow PC$
	RT_1:	$M[AR] \leftarrow TR$, $PC \leftarrow 0$
	RT_2:	$PC \leftarrow PC + 1$, $IEN \leftarrow 0$, $R \leftarrow 0$, $SC \leftarrow 0$
Memory-reference:		
AND	D_0T_4:	$DR \leftarrow M[AR]$
	D_0T_5:	$AC \leftarrow AC \wedge DR$, $SC \leftarrow 0$
ADD	D_1T_4:	$DR \leftarrow M[AR]$
	D_1T_5:	$AC \leftarrow AC + DR$, $E \leftarrow C_{out}$, $SC \leftarrow 0$
LDA	D_2T_4:	$DR \leftarrow M[AR]$
	D_2T_5:	$AC \leftarrow DR$, $SC \leftarrow 0$
STA	D_3T_4:	$M[AR] \leftarrow AC$, $SC \leftarrow 0$
BUN	D_4T_4:	$PC \leftarrow AR$, $SC \leftarrow 0$
BSA	D_5T_4:	$M[AR] \leftarrow PC$, $AR \leftarrow AR + 1$
	D_5T_5:	$PC \leftarrow AR$, $SC \leftarrow 0$
ISZ	D_6T_4:	$DR \leftarrow M[AR]$
	D_6T_5:	$DR \leftarrow DR + 1$
	D_6T_6:	$M[AR] \leftarrow DR$, if $(DR = 0)$ then $(PC \leftarrow PC + 1)$, $SC \leftarrow 0$
Register-reference:		
		$D_7I'T_3 = r$ (common to all register-reference instructions)
		$IR(i) = B_i$ $(i = 0, 1, 2, \ldots, 11)$
	r:	$SC \leftarrow 0$
CLA	rB_{11}:	$AC \leftarrow 0$
CLE	rB_{10}:	$E \leftarrow 0$
CMA	rB_9:	$AC \leftarrow \overline{AC}$
CME	rB_8:	$E \leftarrow \overline{E}$
CIR	rB_7:	$AC \leftarrow$ shr AC, $AC(15) \leftarrow E$, $E \leftarrow AC(0)$
CIL	rB_6:	$AC \leftarrow$ shl AC, $AC(0) \leftarrow E$, $E \leftarrow AC(15)$
INC	rB_5:	$AC \leftarrow AC + 1$
SPA	rB_4:	If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$
SNA	rB_3:	If $(AC(15) = 1)$ then $(PC \leftarrow PC + 1)$
SZA	rB_2:	If $(AC = 0)$ then $PC \leftarrow PC + 1$
SZE	rB_1:	If $(E = 0)$ then $(PC \leftarrow PC + 1)$
HLT	rB_0:	$S \leftarrow 0$
Input-output:		
		$D_7IT_3 = p$ (common to all input–output instructions)
		$IR(i) = B_i$ $(i = 6, 7, 8, 9, 10, 11)$
	p:	$SC \leftarrow 0$
INP	pB_{11}:	$AC(0\text{–}7) \leftarrow INPR$, $FGI \leftarrow 0$
OUT	pB_{10}:	$OUTR \leftarrow AC(0\text{–}7)$, $FGO \leftarrow 0$
SKI	pB_9:	If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$
SKO	pB_8:	If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$
ION	pB_7:	$IEN \leftarrow 1$
IOF	pB_6:	$IEN \leftarrow 0$